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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/981,784
Filing Date: October 19, 2001
Appellant(s): LANGE ET AL.

Nataliya Dvorson
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 3/2/07 appealing from the Office action mailed 7/5/06.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20010034227	SUBRAMANIAN	10-2001
6366607	OZLUTURK	4-2002
6366606	SRIRAM	4-2002

6161024	KOMARA	12-2000
4827499	WARTY	5-1989

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 6-13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram (US 6,366,606) in view of Ozluturk et al. (US 6,366,607).

Regarding claims 1, 9 and 10, Sriram teaches a base station a radio operated telecommunications system with a receiver (col. 1, lines 31-35) for processing received information, and one or more digital signal processors 10 for performing symbol rate processing and a correlator co-processor 12 that performs at least parts of chip rate processing (col. 4, lines 36-41 and col. 5, lines 19-33 and 51-60).

Sriram fails to disclose that the symbol rate processing and chip rate processing is performed by a single processor. However, in an analogous art, Ozluturk discloses a receiver in which a signal processor 67 performs both symbol rate processing and chip rate processing. See FIG. 2, col. 4, lines 1-21 and col. 6, lines 25-37. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Sriram by

performing both symbol rate and chip rate processing in a single processor, as taught by Ozluturk, to eliminate the unnecessary circuit components that previously performed the two kinds of processing, and thereby save space by making the receiver circuitry more compact.

Regarding claims 3, 13 and 21, Sriram fails to specifically teach the signal processor performing chip rate processing before symbol rate processing. However, Ozluturk discloses a system which performs chip rate processing before symbol rate processing. See col. 4, lines 15-21. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform chip rate processing before symbol rate processing, as taught by Ozluturk, so that the information is despread before it is decoded.

Regarding claim 6, Sriram teaches memory which can be suitable for the intermediate storage of the received information (col. 1, lines 45-50 and col. 2, lines 29 and 49-54).

Regarding claim 7, Sriram teaches despreading of the received information by a signal processor (col. 6, lines 34-35).

Regarding claim 8, Sriram teaches decoding of the received information (col. 5, lines 51-60).

Regarding claims 11 and 19, Sriram teaches that the telecommunications system is CDMA (col. 2, lines 18 and 60-67).

Regarding claim 12, Sriram inherently teaches a process for operating a radio-operated telecommunications system, wherein the information received by a base station or a mobile station is subjected to a symbol rate processing by means of a digital signal processor (col. 2, line 34) wherein at least part of the chip rate processing is likewise performed (col. 4, lines 36-41 and col. 5, lines 19-33, 51-60).

3. Claims 2, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram in view of Ozluturk et al. and Warty (US 4,827,499).

Regarding claims 2 and 14, Sriram and Ozluturk fail to teach the signal processor performing task allocation for controlling the chip rate processing and the symbol rate processing. Warty teaches a call control of a distributed processing communications switching system that has processors performing task allocation (col. 5, lines 36-55).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Warty into that of Sriram and Ozluturk for the obvious reason of being able to pick which function to operate for quicker processing because it decentralizes task functionality.

Regarding claim 16, Sriram fails to teach the distribution of the array or group of signal processors between the chip rate processing and the symbol rate processing is performed by task allocation. The limitations of the claim are rejected as the same reason set forth in claims 2 and 14 above, where it would have been obvious to incorporate the teaching of Warty into Sriram because it decentralizes task functionality.

4. Claims 4, 5, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sriram, Ozluturk and Warty as applied to claims 2 and 16 above, and further in view of Komara (US 6,161,024).

Regarding claim 4, Sriram fails to teach an array or group of digital signal processors provided. Komara teaches a redundant broadband multi-carrier base station for wireless

communications with a group of digital signal processors (Fig. 1 and col. 2, lines 63-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Komara into that of Sriram for the obvious reason of having a plurality of processors to accommodate a plurality of users for faster processing and a backup structure for failure purposes.

Regarding claims 5 and 15, Sriram and Komara further teach chip rate processing and symbol rate processing distributed between sub-arrays or sub-groups of signal processors. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to distribute chip rate processing and symbol rate processing between sub-groups order have quicker processing and to reduce complexity of the processors functions.

5. Claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozluturk et al. in view of Subramanian et al (US 2001/0034227).

Regarding claims 20 and 21, Ozluturk discloses a digital signal processor 67 including means for executing symbol rate processing and means for executing chip rate processing, where the digital signal processor is disposed inside a receiver. See FIG. 2, col. 4, lines 1-21 and col. 6, lines 25-37.

Ozluturk fails to disclose means for switching over from the means for executing symbol rate processing to the means for executing chip rate processing, where the digital signal processor is a single digital processor having the symbol rate processing means.

However, in an analgous art, Subramanian discloses coprocessor interface, which is part of a signal processor, that switches between symbol and chip rate processing. See paragraphs 42

and 56. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system in Ozluturk by incorporating these features taught in Subramanian so that the most effective processing can be performed based on the type of processing required at any given time.

Regarding claims 22-24, Ozluturk fails to disclose signal rate processing including decoding the received information and chip rate processing including dispreading the received information based on sources of the received information.

However, Subramanian discloses a configurable spread spectrum device in which signal rate processing including decoding the received information and chip rate processing including dispreading the received information based on sources of the received information. See paragraph 42. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system in Ozluturk and Subramanian by incorporating these further features taught in Subramanian for the purpose of ensuring that the processing is matched to the appropriate sources.

(10) Response to Argument

Examiner respectfully disagrees with Appellant's arguments.

Sriram discloses a programmable correlator co-processor 12 that includes a correlation controller 40 that performs the requested correlations of the requested chips stored in the chip buffer 30 in portions. For example, the co-processor 12 can operate at 16 Ksymbols/second. At 256 chips per symbol, the correlation controller 40 processes each symbol in 32 chip portions. Thus, four cycles are needed to process each symbol. The digital transmissions receiver 10, upon

detection of a symbol in the output buffer 38 then proceeds with its symbol rate processing functions. See FIG. 2 and col. 4, lines 28-42.

The claims of the present application do not define specifically what are "symbols," "chips," "symbol rate processing" and "chip rate processing." Since Sriram teaches that symbols are comprised of chips, given the broadest reasonable interpretation, any device that performs chip rate processing can also be considered to perform symbol rate processing. Therefore, Sriram suggests that the correlation controller automatically performs symbol rate processing when it performs chip rate processing. The digital transmissions receiver 10 merely performs additional processing on each symbol separately. Also, the chip rate processing is shown as being performed before the symbol rate processing, even though the order of processing is not significant.

Moreover, since Sriram already discloses the structure for performing both symbol rate processing and chip rate processing, it would be obvious to integrate the functions the digital transmissions receiver 10 and the co-processor 12 into a single device. The use of a one piece construction for performing both types of procesing, instead of the structure disclosed in Sriram, would be merely a matter of obvious engineering choice. See *In re Fridolph*, 50 CCPA 745, 89 F.2d 509, 135 USPQ 319.

Ozluturk clearly teaches this one-piece construction by disclosing a receiver in which a signal processor 67 performs both symbol rate processing and chip rate processing. See FIG. 2, col. 4, lines 1-21 and col. 6, lines 25-37. In these passages, Ozluturk discloses that carrier offset correction is performed at the symbol level and the chip level by the signal processor. Since the symbol rate is much less than the chip rate, less overall processing speed is required when

correction is done at the symbol level. There are no channel despreaders in the embodiment shown in FIG. 2 and therefore both symbol rate and chip rate processing is performed by the single signal processor 67. In other embodiments also, such as those shown in FIGS. 12 and 13, the symbol and chip rate processing is performed by the single processing unit 157. See col. 7, lines 15-29.

The motivation for combining of Sriram and Ozluturk is to eliminate the unnecessary circuit components that previously performed the two kinds of processing, and thereby save space by making the receiver circuitry more compact. This goal is achieved by the combination because Ozluturk has a single processor that performs both symbol rate processing and chip rate processing where these separate functions were previously performed by two respective processors.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Regarding claim 5, Komara discloses that the DSPs 18 are split into groups each programmed to demodulate each channel signal 15 as specified by the air interface standard supported by the base station 10. There typically is not a one-to-one correspondence between the number of DSP demodulators 18 and the number of channel signals, n, provided by the

channelizers 14 in each transceiver 31-34. For example, the DSP's may each process a number, such as 24, of digital channel signals 15 at the same time. See FIGS. 1 and 2 and col. 4, lines 35-42. The combination of Sriram, Ozluturk, Warty and Komara teaches chip rate processing and symbol rate processing distributed between sub-arrays or sub-groups of signal processors.

Regarding claim 23, Ozluturk is not relied upon for teaching a processor separating the received information based on sources of the received information and assigning the separated received information to a respective source. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Subramanian discloses a configurable spread spectrum device in which signal rate processing including decoding the received information and chip rate processing including dispreading the received information based on sources of the received information. See paragraph 42, lines 1-27.

Subramanian also discloses a coprocessor interface, which is part of a signal processor, that switches between symbol and chip rate processing. See paragraphs 42 and 56. Subramanian is not relied upon for teaching a single processor to perform all of the chip rate processing, the symbol rate processing, and the switching, and transmission of information in the digital processor first to the means for executing chip rate processing and then to the means for executing symbol rate processing. Rather, the combination of Ozluturk and Subramanian teaches these features. Once again, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. The motivation for

the combination of Ozluturk and Subramanian is to perform the most effective processing based on the type of processing required at any given time. There is no reason why an external computing device of Subramanian cannot be placed in the processor of Ozluturk. Processing matched to appropriate sources means that decoding is done by a signal rate processor and dispreading is done by the chip rate processor.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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